

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Robert B. Staszewski, et al.

Serial No.: **09/695,516**

Filed: **10/24/00**

For: **HYBRID OF PREDICTIVE AND CLOSED-LOOP PHASE DOMAIN
DIGITAL PLL ARCHITECTURE**

Docket No.: **TI-30674**

Examiner: **Kinhead**

Art Unit: **2817**

Confirm. No.: **3115**

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AMENDMENT - 37 C.F.R. § 1.111

10/16/2002 PWALKER 00000003 200668 09695516

01 FC:1201 Assistant Commissioner for Patents

Washington, D.C. 20231

CERTIFICATION OF FAX TRANSMITTAL

I hereby certify that the above correspondence is being facsimile transmitted to the United States Patent and Trademark Office on September 17, 2002.


Elizabeth Austin

Adjustment date: 10/18/2002 PWALKER
09/24/2002 WABDELRL 00000027 200668 09695516
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Responsive to the Office Action dated May 22, 2002, please amend the above-identified application, as set forth below.

IN THE CLAIMS – (clean copy):

1. (amended) A digital phase-domain phase-locked loop circuit comprising:
a digitally-controlled oscillator (DCO);
a gain element feeding the DCO and operational to compensate for DCO gain in response to
a phase accumulator operational to accumulate DCO generated clock edges.